Form PTO-1449 (Rev. 8-83)	U.S. Department of Commerce Patent and Trademark Office	Atty Docket 0756-2158	Serial No. 09/542,473
INFORMATION DISCLOSURE STATEMENT		Applicants: Takayuki IKEDA	
		Filing Date: April 04, 2000	Group Art Unit: 2826

U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date (if appropriate)
A.S.	6,013,929	01/11/2000	Ohtani			

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner Initial	
A.S.	Specifications and Drawings for Application Serial No. 08/862,895, "Semiconductor Intergrated Circuit and Fabrication Method Thereof", Filing Date: May 23, 1997, Inventor: Hisashi OHTANI
A.S	Specifications and Drawings for Application Serial No. 09/468,859, "Thin Film Transistor, Method of Manufacturing the Same, and Semiconductor Device Including the Same" Filing Date: December 21, 1999, Inventor: Hisashi OHTANI
	Specifications and Drawings for Application Serial No. 09/487,432, "Semiconductor Device and Process for Production Thereof" Filing Date: January 19, 2000, Inventors: Shunpei YAMAZAKI et al.
	Specifications and Drawings for Application Serial No. 09/493,411, "Semiconductor Device and Method of Fabricating the Same" Filing Date: January 28, 2000, Inventors: Shunpei YAMAZAKI et al.

Examiner A.S	Date Considered 5/18/03

*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this formwith next communication to applicant.